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TITLE

METHOD AND SYSTEM FOR CLOCK SYNCHRONIZATION OF SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a clock synchronization mechanism, more particularly to a method and system for clock synchronization of semiconductor devices, which uses a master-slave configuration in conjunction with a phase checker, such that semiconductor devices synchronize the clocks and thus precisely output clock demands to ensure reliability during operation.

Description of the Related Art

At present, for clock synchronization, most designs focus on a single chip, as described in USP 5,999,025 and USP 6,304,582. The former (USP 5, 999, 025) essentially describes a synchronization of an external clock and an on-chip voltage controlled oscillator (VCO) clock. The latter (USP 6,304,582) essentially describes a synchronization of an oscillator clock and clocks in a chip. As cited, these clock synchronization means for multiple chips lack effectiveness with semiconductor devices in which delay locked loop (DLL) or digital clock manager (DCM) is used as a clock source.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a method and system for clock synchronization of semiconductor

devices, which uses a master-slave configuration to align all clock sources from delay locked loops (DLLs) or digital clock managers (DCMs), such that semiconductor devices synchronize the clocks and thus precisely output clock demands to ensure reliability during operation.

The present invention is generally directed to a method and system for clock synchronization of semiconductor devices, which uses a master-slave configuration to designate one semiconductor device with the lowest rate clock as a master element and other semiconductor devices as slave elements, use a phase checker in the master element to calibrate all clocks of the master element, use an external phase checker to respectively synchronize clocks in corresponding slave elements with the lowest rate clock and use an internal phase checker to respectively synchronize all clocks in the slave elements, thereby accurately outputting clocks required by circuits inside the semiconductor devices.

DESCRIPTION OF THE DRAWINGS

The present invention will be described by way of exemplary embodiments, but not limitations, illustrated in the accompanying drawings in which like references denote similar elements, and in which:

Fig. 1 is a block diagram of a clock synchronization of semiconductor devices with a master-slave configuration according to the invention;

Fig. 2 is a block diagram of the interior of a master element of Fig. 1 according to the invention;

Fig. 3 is a block diagram of the interior of a slave element of Fig. 1 according to the invention;

Fig. 4 is a block diagram of the interior of a delay locked loop (DLL) clock generator according to Fig. 2 or 3 of the invention;

Fig. 5 is an example of a phase checker according to the invention;

Fig. 6 is a timing of an external phase checker according to the invention;

Fig. 7 is a timing of an internal phase checker according to the invention;

Fig. 8 is a flowchart of an operating method according to the invention;

Fig. 9 is a flowchart of a synchronization of clock sources inside the master element according to Fig. 8 of the invention;

Fig. 10 is a flowchart of a clock synchronization between the master and slave elements according to Fig. 8 of the invention; and

Fig. 11 is a flowchart of a synchronization of clock sources inside the slave elements respectively according to Fig. 8 of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 is a block diagram of a clock synchronization of semiconductor devices with a master-slave configuration according to the invention. In this case, four Field Programmable Gate Arrays (FPGAs) are embodied, without limiting the embodiment, for better explanation. For

example, ten Application Specific Integrated Circuits (ASICs) can be used.

As shown in Fig. 1, each Field Programmable Gate Array (FPGA) includes two major functional blocks, respectively to phase checkers 111, 121, 131, 141 and clock generators 112, 122, 132, 142. Each clock generator 112, 122, 132, or 142 internally include delay locked loops (DLLs) or digital clock managers (DCMs) as required clocks. Each phase checker checks rising or falling edges of the clocks for alignment. If any clock is not aligned, a reset is issued. In this case, reset signals reset11-reset14 are output to reset corresponding clock generators for clock re-generation. For clock synchronization, a master-slave configuration is implemented by designating a semiconductor device with the lowest rate clock as a master element, in this case, 11, and other semiconductor devices as slave elements, in this case, 12-14. After other clocks in the master element are calibrated by the lowest rate clock (zeroing), all clocks in the slave elements are synchronized respectively by a reference clock CLKREF from the master element. The cited clock calibration and synchronization are further described in connection with delay locked loops (DLLs).

Fig. 2 is a block diagram of the master element 11 of Fig. 1. In Fig. 2, the element 11 has a clock generator consisting of multiple DLLs. As shown in Fig. 2, in the master element 11, at first, zeroing is performed by a phase checker to check if all rising or falling edges of clock sources CLKREF and $clkf_1$-$clkf_n$ are aligned. If any edge is not aligned, the phase checker 111 sends a reset signal

reset11 such that the clock generator 112 re-generates clock sources until clock sources are aligned on every rising or falling edge. At this point, zeroing is complete and an aligned clock Phase-OK is sent by the phase checker 111. Additionally, the lowest clock source aligned is referred to as a reference clock source CLKREF and sent to the phase checker 121, 131 and 141 for calibrating slave devices. The clock sources are thus synchronized when the slave devices are calibrated by means of the source CLKREF. Other clock sources are applied in use of internal circuit 10 connecting with a respective slave FPGA.

Fig. 3 is a block diagram of an internal circuit of any slave device according to Fig. 1 of the invention. In Fig. 3, any slave device 12, 13 or 14 includes a clock generator 33 formed by a plurality of DLLs all devices, and a phase checker 121, 131 or 141 formed by an external checker 31 and internal phase checkers 32. As shown in Fig. 3, any slave device 12, 13 or 14 has two checkers 31, 32. The external phase checker 31 first synchronizes a local lowest clock source $clkf_{lowest}$ and the lowest clock source CLKREF and then sends a calibrated signal Phase-In-OK to the internal phase checker 32. The internal phase checker 32 aligns other clock sources $clkf_1$-$clkf_n$ based on the calibrated signal Phase-In-OK and results in clock synchronization. Therefore, all clock sources generated by the DLLs are accurately provided to next FPGA internal circuits. However, if the local lowest clock source $clkf_{lowest}$ does not synchronize with the lowest clock source CLKREF, the external phase checker 31 sends a reset signal Reset31 to a clock generator 331 with the local lowest clock source

$clkf_{lowest}$ to re-generate required clock signals. If the signal Phase-In-OK does not synchronize with the local clock sources $clkf_1$-$clkf_n$, the internal phase checker 32 sends a reset signal Reset32 to clock generators 332 with the local clock sources to re-generate required clock signals.

Fig. 4 is a block diagram of a DLL interior in Figs. 2 and 3. As shown in Fig. 4, the DLL essentially includes a variable delay line 41, a clock distribution network 42 and a control logic 43. The variable delay line 41 delays an external input clock CLK for a certain time and then outputs a resulting clock CLKOUT. The network 42 converts the clock CLKOUT into required rate clock sources Base-fn for corresponding circuits and a feedback signal CLKFB is sent to the control logic 43. The control logic 43 compares rising edges of the signals CLK and CLKFB to determine if all edges of the signals CLK and CLKFB are aligned. The comparison result CMP is sent to the delay line 41 for adjustment until the alignment is complete and the DLL is locked. As such, the clock delay effect between the input clock CLK and the load is eliminated, so clock synchronization is obtained. The variable delay line can be a voltage controlled delay.

Fig. 5 is an example of a phase checker according to the invention. In Fig. 5, for simple description, the phase checker only has two D-type flip-flops (D-FFs) 51, 52 and a finite state machine (FSM) 53. In practice, the D-FF number used depends on required clock frequencies, generally with one-to-one relation. As shown in Fig. 5, when clock line is logic 0, a clock signal fn and a lowest clock signal f_{lowest} are respectively transmitted to the devices 51, 52 to output

sampling signals CLKSAMPLE1, CLKSAMPLE2 to the device 53 for phase check. In the phase checker of the master device, the lowest clock signal f_{lowest} represents the signal CLKREF and the signal phase-ok represents the zeroing signal Phase-OK. In the external phase checker of a slave device, the lowest clock signal f_{lowest} represents the signal CLKREF and the signal phase-ok represents the calibrating signal Phase-In-OK. In the internal phase checker of the slave device, the lowest clock signal f_{lowest} represents the local lowest clock signal $clkf_{lowest}$ of the slave device and the signal phase-ok represents the zeroing signal Phase-OK. In the following, further description of timings of external and internal phase checkers is given.

Fig. 6 is a timing diagram of the external phase checker of a slave device. Fig. 7 is a timing diagram of the internal phase checker of the slave device. As shown in Fig. 6, in each falling edge of input clock signal CLK, the external phase checker synchronously checks each pair of falling edges of the lowest clock signals (circle mark) CLKREF, $clkf_{lowest}$ of the master device and the slave device to determine if the two have the same value. If not, a reset signal Reset is sent to re-input the two lowest clock signals for re-alignment. Two lowest clock signals having the same value indicates that the master device 11 is calibrated or the slave devices connected to the master device 11 are aligned. At this point, as shown in Fig. 7, the external checker refers to the local lowest clock signal (aligned $clkf_{lowest}$) as an aligned signal Phase-In-OK, inputting to the internal phase checker to perform aligning steps described in Fig. 6. Thus, all local clock sources

required by the internal circuits of the Field Programmable Gate Array (FPGA) are aligned, in this case, f_1-f_3, to obtain clock synchronization of all semiconductor devices.

Fig. 8 is an operating flowchart of the invention. As shown in Fig. 8, multiple clock sources are generated by clock generators inside a plurality of semiconductor devices (S1). When the multiple clock sources are stable, one semiconductor device having a clock source with the lowest rate clock signal is designated as a master device and other devices are designated as slave devices (S2). The lowest rate clock signal of the master device is designated as a reference clock source (S3). According to the reference clock source, a phase-aligned check is performed on other clock sources in the master device, such that other clock sources of the master device are synchronized with the reference clock source to generate a zeroing signal (S4). According to the zeroing signal, a phase-aligned check is respectively performed on a local lowest rate clock source in each slave device, such that all local lowest rate clock sources of the slave devices are synchronized with the lowest rate clock signal of the master device to respectively generate an aligning signal (S5). According to the aligning signal, a phase-aligned check is respectively performed on other clock sources in each slave device, such that other clock sources of each slave device are separately synchronized with the local lowest rate clock signal of the respective slave devices (S6). Therefore, clock synchronization for the plurality of semiconductor devices is complete.

Step S4 is further divided into the steps of Fig. 9, including that by means of rising or falling edges of an external input clock source, a phase checker in the master device is triggered to sample the clock sources inside the master device for phase alignment comparison (S41); when all phases are aligned, the signal Phase-OK is output to concurrently signal each slave device (S42); and otherwise, a reset signal reset is output to re-generate multiple clock sources for re-alignment operation (S43).

Step S5 is further divided into the steps of Fig. 10, including that an external phase checker in each slave device respectively checks the lowest rate clock source of the master device to determine if the zeroing signal has been sent (S51); when the zeroing signal is received and all clock sources in each slave device are stable, each external phase checker performs a phase-aligned check on its respective slave device (S52); when all phases are aligned, the aligning signal Phase-In-OK is respectively sent to indicate a phase alignment and clock synchronization for the lowest rate clock signal of the master device and the local lowest rate clock signal of the respective slave device (S53); and otherwise, a reset signal reset is sent to re-generate the local lowest rate clock signal of the respective slave device and then repeat the aforementioned steps (S54).

Step S6 is further divided into the steps of Fig. 11, including, when the aligning signal is received and all clock sources in each slave device are stable (S61), an internal phase checker in each slave device performing the phase-aligned check on its respective slave device (S62);

when all phases are aligned, the aligning signal Phase-In-OK is sent to indicate a phase alignment for the clock sources in the respective slave device and of the clock synchronization for the semiconductor devices (S63); and otherwise, a reset signal reset is sent to respectively re-generate the multiple clock sources, except the local lowest rate clock source, of the respective slave device and then repeat the aforementioned steps (S64).

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.